REMARKS

Applicants greatly appreciate Examiner Portka's willingness to conduct a telephone interview with the undersigned attorney on July 24, 2002 and with Dr. Lee, Ms. Toth, and the undersigned attorney on July 25, 2002. The following paragraphs contain a summary of the substance of those interviews.

I. Introduction

In this Amendment, Applicants have canceled Claims 104, 106, 107, 109, 111, and 112 without prejudice. Applicants reserve the right to pursue the subject matter of the cancelled claims in a continuation application. After this amendment, Claims 114-124 remain pending. The independent claims (Claims 114, 117, and 120) each recite a memory comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another ***in a single chip***. Each of these claims was rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,208,545 to Leedy. As discussed during the telephone interviews, Leedy fails to anticipate Claims 114-124 because Leedy does not teach a plurality of memory layers stacked vertically above one another ***in a single chip***. Instead, Leedy merely teaches a module comprising a stack of individual chips. Accordingly, Applicants respectfully request reconsideration and withdrawal of the § 102(e) rejections of Claims 114-124.

II. The Well-Known and Recognized Meaning of "Chip"

A chip is a monolithic integrated circuit that has all of its components manufactured together in situ, as compared to a stack of individual integrated circuits assembled after manufacturing. Applicants have attached several references to show that this meaning of "chip" is well-known and recognized in the art. Several of these references describe the history of the chip and how its inventor, Jack Kilby, developed the chip to eliminate the problems associated

with an assembled stack of individual components — the same type of module disclosed in Leedy. The following passages are excerpts from those references.

> [TI] developed a prototype that ran wires through a stack of miniature components that were stacked vertically . . . . [Kilby] decided to try things his way . . . . By manufacturing all pieces together, Kilby believed, there would be no need to wire anything together since all the connections would go inside the chip. And, by eliminating the wiring and the connections, many components could be included on one chip. On July 24, 1958, Kilby wrote in his lab notebook what would come to be known as ***The Monolithic Idea***. It stated that circuit elements such as resistors, capacitors, distributed capacitors and transistors, if all made of the same material, could be included ***in a single chip***.[1]

> Jack Kilby's invention of the ***Monolithic Integrated Circuit*** was conceptually simple, technically challenging, and socially pervasive. . . . By manufacturing all pieces together inside the ***chip***, he theorized, separate parts could be spared post production hand wiring, and more parts could be implanted. On July 24, 1958, Kilby wrote his ***Monolithic Idea*** into his lab notebook. Circuit elements, if all made of the same material, could be fabricated as part ***of a single chip***.[2]

> The successful invention — The Monolithic Idea — resolved the tyranny of numbers by reducing the numbers to one: a complete circuit would consist of one part — a single ("monolithic") block of semiconductor material containing all the components and all the interconnections of the most complex circuit designs. ***The tangible product of that idea, known to the engineers as the monolithic integrated circuit and to the world at large as the semiconductor chip***, has changed the world . . . .[3]

> "Further thought led me to the conclusion that semiconductors were all that were really required - that resistors and capacitors [passive devices], in particular, could be made from the same material as the active devices [transistors]. I also realized

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[1] "Jack St. Clair Kilby," Jones Telecommunications & Multimedia Encyclopedia, http://www.digitalcentury.com/encyclo/update/kilby.html, ¶¶ 9-10 (1999) (emphasis added) (Tab A).

[2] "The 'Chip' Inventors (part 1)," Dan Murray, http://www.livingstonmontana.com/ access/dan/150thechipinventors-1.html, ¶¶ 1 and 10 under the "Kilby" heading (1999) (emphasis added) (Tab B).

[3] T. R. Reid, "The Chip: How Two Americans Invented the Microchip and Launched a Revolution," page 23 (1984) (emphasis added) (Tab C).

that, since all of the components could be made of a single material, they could also be made in situ interconnected to form a complete circuit," Kilby wrote in a 1976 article titled "Invention of the IC." [4]

Other references illustrate the link between the terms "chip" and "integrated circuit," which is relevant to col. 3, line 2 of Leedy, which states that the Leedy invention is a stacked 3D circuit assembly technology.

> ***integrated circuit*** (IC): An electronic circuit that consists of many individual circuit elements, such as transistors, diodes, resistors, capacitors, inductors, and other active and passive semiconductor devices, ***formed on a single chip*** of semiconducting material and mounted on a single piece of substrate material. ***Synonyms chip*** (def.#1), microcircuit.[5]
>
> The truly distinctive features of the circuits produced by these technologies are: a) inseparability of circuit elements, b) embodiment on a common substrate, and c) fabrication in situ.[6]
>
> In particular, edges of an area on the wafer called a die or a chip are typically aligned in directions along which the wafer readily breaks so that the dice can be separated from one another.[7]
>
> After this preliminary functional testing[,] the wafer is diced into individual circuits or chips . . . .[8]

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[4] "About Jack" http://www.ti.com/corp/docs/kilbyctr/jackbuilt.shtml, second paragraph after the "Enter Kilby" subheading (2002) (Tab D).

[5] "Definition: integrated circuit," http://www.its.bldrdoc.gov/fs-1037/dir-019/_2755.htm (1996) (emphasis added) (Tab E).

[6] Meindl, "Definitions of Terms for Integrated Electronics," IEEE Journal of Solid-State Circuits, item 3, page 2 (March 1967) (Tab F).

[7] Muller et al., "Device Electronics for Integrated Circuits," page 65 (Second edition 1986) (Tab G).

[8] Id. at 106 (Tab G).

In conclusion, as shown by the above references, "chip" is well-known and recognized in the art as referring to a monolithic integrated circuit that has all of its components manufactured together in situ.

III. Leedy Does Not Teach Memory Layers Stacked in a Single Chip

Leedy discloses a stacked integrated circuit memory — **not** a chip, as recited in the claims. Leedy states that his "invention relates to ***stacked integrated circuit memory***" (col. 1, lines 9-10; emphasis added) and defines his 3DS (Three Dimensional Structure) memory device as a ***stack of integrated circuit layers bonded together*** with fine-grain vertical interconnects (col. 3, line 66 – col. 4, line 12). Leedy makes clear that this stack of integrated circuits is a stack of individual chips: "[t]he 3DS circuit may be considered a vertically assembled MCM (***Multi-Chip*** Module)." Col. 11, lines 21-22 (emphasis added). During the telephone interview, the Examiner stated that the rejections would have to be withdrawn if Leedy used the word "is" instead of the word "may" to relate his 3DS circuit and a stack of chips. Upon further review of Leedy, Applicants note that Leedy indeed defines his 3DS circuit to be a stack of chips: "The present 3DS memory technology ***is a stacked or 3D circuit assembly technology***." Col. 3, lines 1-2 (emphasis added).

Additionally, Leedy clearly distinguishes his stacked memory structure from a monolithic integrated circuit, or chip:

> The present invention furthers, among others, the following objectives: 1. Several-fold lower fabrication cost per megabyte of memory ***than circuits conventionally made solely with monolithic circuit integration methods***. Col. 2, lines 48-52 (emphasis added).
>
> This is significantly less ***than that presently experienced in monolithic DRAM circuit designs*** where the percentage of non-memory cell area can exceed 40%. Col. 6, lines 8-11 (emphasis added).

> The 3DS memory device decouples control functions ***that normally would be found adjacent the memory cells of monolithic memory circuits*** and segregates them to the controller circuit. Col. 6, lines 14-17 (emphasis added).

In summary, Leedy merely discloses a stack of individual integrated circuits assembled after manufacturing — not a chip, as recited in the claims.

IV. Conclusion

The 35 U.S.C. § 102(e) rejections of Claims 114-124 based on Leedy should be withdrawn because Leedy fails to teach a memory comprising a plurality of memory cells arranged in a plurality of layers stacked vertically above one another in a single chip, as recited in the claims. Leedy merely discloses a stack of individual integrated circuits assembled after manufacturing.

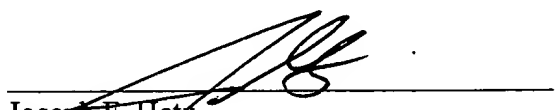
In view of the foregoing amendments and remarks, Applicants submit that the present application is in condition for allowance. Reconsideration is respectfully requested.

V. Request for Interview

Applicants respectfully request that the Examiner contact the undersigned attorney at (312) 321-4719 to schedule a telephone interview to discuss this Amendment.

Dated: July 26, 2002

Respectfully submitted,



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